Amendments to the Claims

This listing of the claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A communication system for providing high speed communications between a first location and a second location, said communication system comprising:

~~a first clock resident or derived at said first location, said first clock related to a transmission rate~~;

~~a second clock related to a network link rate~~;

a transmitter module at the first location associated with a first clock, the transmitter module comprising a phase ~~device~~ detector module operable to generate a one or more data bits to indicate phase ~~error signal~~ offset between the first clock and a second clock, the first clock to be to be associated with ~~as a function of said~~ a transmission rate and ~~said~~ the second clock to be associated with a network link rate;

a receiver module at the second location associated with the second clock, the receiver module to be coupled to ~~a network coupling a~~ the transmitter module via a network ~~at said first location to a receiver present at said second location~~;

wherein said transmitter module is operable to transmit to said receiver module ~~both~~ at least one of a data stream ~~synchronized with said network link rate~~ and ~~said~~ the one or more data bits to indicate phase ~~error signal~~ offset via the network; and

wherein said receiver module is operable to ~~recover~~ determine ~~an estimate of said~~ the transmission rate associated with the first clock at the first location ~~as a function of said~~ based on the one or more data bits to indicate phase ~~error signal~~ offset and said network link rate.

2. (Currently Amended) A communication system as recited in claim 1, wherein said first clock and said second clock have a predefined relation, and said phase ~~device~~ detector module is operable to generate signals from said first and said second clocks, said signals having a nominal frequency rate rendering phase comparison of said first and said second clocks possible.

3. (Cancelled)

4. (Currently Amended) A communication system of claim 1, wherein said transmitter module is operable to transmit said one or more data bits to indicate phase ~~error signal~~ offset in an overhead channel.

5. (Currently Amended) A ~~transmitter circuit~~ timing generation module for use in a data communications system, said timing generation module ~~transmitter circuit operable to transmit data at a synchronized rate, said transmitter circuit~~ comprising:

a first variable modulus counter having a first clock input, a first control input, and a first variable modulus counter output, said first clock input ~~intended for coupling~~ to be coupled to a transmitter clock, said first variable modulus counter ~~controllable~~ operable to divide ~~the frequency of~~ the transmitter clock frequency by a first adjustable integer ~~adjustable by an arbitrary integer offset +/ N~~;

a second variable modulus counter having a second clock input, a second control input, and a second variable modulus counter output, said second clock input ~~intended for coupling~~ to be coupled to a network link clock, the ~~frequency of said~~ network link clock frequency having a predetermined relationship ~~to~~ with ~~the frequency of~~ the transmitter clock frequency, said second variable modulus counter ~~controllable~~ operable to divide the ~~frequency of the =~~network link clock frequency by a second adjustable integer ~~adjustable by an arbitrary integer offset +/ M~~;

wherein said first adjustable integer is selected to a first value and the second adjustable integers ~~are~~ is selected to be a second value such that the quotient of the transmitter clock frequency divided by the first value is substantially the same as the quotient of the network link clock frequency divided by the second value ~~outputs of said first and said second variable modulus counters have an identical nominal frequency~~,

a ~~detector~~ phase detector module comprising one or more D flip-flops, the phase detector module couple-able to the first clock input and the second clock input to generate one or

more data bits to indicate a phase offset between the first clock input and the second clock input; and

~~having a first input coupled to said first output, a second input coupled to said second output, and a detector output, said detector operable to generate a phase error signal reflective of a phase difference between said signals generated at said first and second outputs; and~~

a modulus control ~~circuit~~ module responsive to one or more data bits to indicate a phase offset ~~said phase error signal~~ to control said first and second variable modulus counters.

6-7. (Cancelled)

8. (Currently Amended) A timing generation module ~~transmitter circuit~~ as recited in claim ~~7~~5, wherein said transmitter ~~circuit~~ module is further operable to transmit data at a rate substantially synchronized with said network link clock frequency.

9. (Currently Amended) A timing generation module ~~transmitter circuit~~ as recited in claim 8, wherein said network link clock is further operable to transmit said quantized bit in an overhead channel.

10-11. (Cancelled)

12. (Currently Amended) A ~~transmitter circuit~~ timing generation module as recited in claim 5, wherein said transmitter circuit is one component of a high speed modem.

13. (Currently Amended) A receiver circuit for use in a data communications system, said receiver circuit operable to receive data and to recover transmit timing data and synchronize received data according to recovered transmit timing data, said receiver circuit comprising:

a first variable modulus counter controllable to frequency divide a first input signal by a first integer adjustable by an arbitrary integer offset +/-N to generate a first output signal;

a second variable modulus counter controllable to frequency divide a second input signal by a second integer adjustable by an arbitrary integer offset +/-M to generate a second output signal;

a detector circuit operable to determine a phase relation between said first and second output signals;

an oscillator circuit controlled by said phase relation, said oscillator providing feedback to said second variable modulus controller;

a modulus control circuit responsive to received timing data, said modulus control circuit operable to control said first and second variable modulus counters,

whereby said receiver circuitry reaches a steady state and generates a clock signal for synchronizing received data ~~around~~ based on recovered phase variation information.

14. (Currently Amended) A receiver circuit as recited in claim 13 further comprising:

circuit~~ry~~ for receiving primary transmitted data; and circuit~~ry~~ for recovering received timing data ~~from within an overhead channel~~.

15. (Currently Amended) A receiver circuit as recited in claim 13 further comprising:

a lowpass filter coupled between said ~~phase~~ detector circuit and said oscillator circuit.

16. (Currently Amended) A method, ~~for timing~~ of signal generation ~~and recovery in a communications system requiring synchronization~~, the method comprising:

providing a master clock signal and a network link clock signal ~~at a transmitter~~; ~~calculating~~ determining a phase relation between said master clock signal and said network link clock signal; and

~~via said transmitter, transmitting data to a receiver at first rate specified by said network link clock signal; and~~

re-generating the master clock signal based on the phase relation and the network link clock signal.

~~via said transmitter, transmitting said phase relation to said receiver.~~

17. (Cancelled)

18. (Currently Amended) A method ~~for timing generation and recovery in a communications system~~ as recited in claim 16, wherein:

~~calculating~~ the determining said phase relation includes quantizing said phase relation; and

said providing the quantized phase relation ~~is transmitted~~ via an overhead channel.

19. (Currently Amended) A method as recited in claim 16, wherein said master clock signal and said network link clock signal have a ~~fixed~~ predetermined relation defined by a first adjustable integer and a second adjustable integer, wherein ~~calculating~~ the determining said phase relation includes:

determining a first value for the first adjustable integer and determining a second value for the second adjustable integer such that the quotient of a master clock signal frequency divided by the first value is substantially the same as the quotient of a network link clock signal frequency divided by the second value;

~~frequency~~ dividing said master clock signal frequency by the first value ~~(said first integer plus a phase correction +/-N) in order~~ to generate a first signal of a first frequency ~~substantially a nominal rate~~;

~~frequency~~ dividing said network link clock signal frequency by the second value ~~(said second integer plus a phase correction +/-M) in order~~ to generate a second signal of a second frequency ~~substantially a nominal rate~~; wherein the first frequency and the second frequency are substantially equal to a reference frequency value;

~~determining said phase relation by~~ compar~~ingson of~~ said first signal with said second signal to determine the phase relation; and

~~determining~~ adjusting ~~said phase corrections +/-N and +/-M~~ one or more of a value of the first adjustable integer and a value of the second adjustable integer ~~in an ongoing fashion~~ based on the phase relation.

20. (Original) A method as recited in claim 19, wherein said phase relation is quantized.

21. (Currently Amended) A method as recited in claim 19, wherein said phase relation is transmitted via an overhead channel at a frequency ~~equal to or lower~~ no larger than ~~said nominal rate~~ the reference frequency value.

22. (New) The timing generation module of claim 5, further comprising a phase accumulator module coupled to an output of the phase detector module.

23. (New) The timing generation module of claim 22, further comprising a register having an output port to be coupled to an input port of the phase accumulator module, the register to be adjustable to determine a phase offset correction resolution.

24. (New) The timing generation module of claim 22, wherein the phase accumulator module is coupled to a delta-sigma modulator.